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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/494,787	01/31/2000	John A. Mount	SEA9274	3950

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EXAMINER	
SORRELL, ERON J	
ART UNIT	PAPER NUMBER
2182	

MAIL DATE	DELIVERY MODE
02/07/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MW

Office Action Summary	Application No.	Applicant(s)	
	09/494,787	MOUNT, JOHN A.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-14* is/are allowed.

6)☒ Claim(s) *1-5 and 15-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Examiner's Remarks

1. Applicant's amendment to the claims and remarks are sufficient to overcome the outstanding the outstanding 25 USC 112 1st and 2nd paragraph rejections set forth in the Office Action Mailed 9/12/07.

Drawings

2. The drawings were received on 11/21/07. These drawings are acceptable.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3,5,16,18, and 21-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Asano et al. (U.S. Patent No. 5,457,787 hereinafter "Asano").

5. Referring to claims 1,16, and 21, Asano teaches in an apparatus (see figure 1) having a bus (see item 16 in figure 1) operatively coupled to a first controller chip (see item 18 in figure 1) and a first channel chip (see item 14 in figure 1), the channel chip having several registers (see figure 2), the apparatus also having a storage medium operatively coupled to the bus through a storage medium interface (see lines 39-45 of column 3), a method for retrieving data recorded on the storage medium comprising steps of:

(a) retrieving a first portion of the recorded data via the bus (see lines 44-51 of column 4);

(b) updating some of the registers via the bus (see 21-25 of column 4); and

(c) retrieving a second portion of the recorded data via the bus (see lines 44-51 of column 4). Note that step (a) may be the completion of a first read command, step (b) sets the parameters for a subsequent read command, and step (c) is the start of the subsequent read command. Note also that data is read over bus 16 and the registers are updated via bus 16.

6. Referring to claim 2, Asano teaches the interface includes a read head (see item 20 in figure 1), further comprising a step

(d) of repositioning the storage medium interface with respect to the storage medium, between retrieving steps (a) and (c) (see lines 46-64 of column 3).

7. Referring to claim 3, Asano teaches the interface has a plurality of operating parameters that are modified in updating step (b) (see lines 46-64 of column 3).

8. Referring to claim 5, Asano teaches the registers contain at least one mode-indicative value. (see lines 52-63 of column 4, note Asano teaches a pre-read and post-read mode).

9. Referring to claims 18 and 22, Asano teaches the bus is at least a parallel bus (see item 16 in figure 2).

10. Referring to claim 23, Asano teaches the first and second data are user data (see lines 44-63 of column 4).

11. Referring to claim 24, Asano teaches the user data is transmitted via the bus between the read/write channel and a controller (see bus connecting items 18 and 28 in figure 1).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano in view of Du et al. (U.S. Patent No. 6,381,085 hereinafter "Du").

14. Referring to claim 4, Asano fails to teach the registers contain at least one read channel parameter value selected from the group consisting of: a precompensation value, a filter coefficient value, and a phase offset value.

Du teaches in an analogous system, registers containing a read channel parameters comprising at least a filter coefficient value (see lines 21-35 of column 2).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system and method of Asano with the above limitation of Du. One of ordinary skill in the art would have been motivated to make

such modification because Du suggests this parameter helps improve the bit error rate (see lines 21-35 of column 2).

15. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano in view of O'Brien et al. (U.S. Patent No. 3,883,853 hereinafter "O'Brien").

16. Referring to claim 17, Asano fails to teach the bus is a serial bus.

O'Brien teaches, in an analogous system, the bus being a serial bus (see data bus in figure 3).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Asano such that the bus is a serial bus to reduce the overall cost of the system.

17. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano in view of Hessing et al. (U.S. Patent No. 5,276,564 hereinafter "Hessing").

18. Referring to claim 25, Asano teaches the method of claim 21, however Asano fails to teach the first and second data are transmitted at different data rates.

Hessing teaches, in an analogous system, the above limitation (see lines 1-13 of column 2).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the teachings of Asano with the above teachings of Hessing in order to account for the difference in the location of data on the storage medium as suggested by Hessing (see lines 1-13 of column 2).

19. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano in view of Taniai et al. (U.S. Patent No. 5,438,665 hereinafter "Taniai").

20. Referring to claim 15, Asano teaches an apparatus (see figure 1) comprising:

an interface configured to read data from a storage medium (see item 20 in figure 1);

a memory containing several values indexed by zone identifiers (see lines 44-51 of column 4);

a first controller chip containing a microprocessor (see item 18 in figure 1);

a first channel chip having several registers (see item 18 in figure 1 and the detailed diagram of item 18 in figure 2); and

a bus operatively coupled between the interface and the chips, the bus controllable to read from the memory and to update several of the registers in response to a zone transition event (see item 16 in figure 1). Note that step (a) may be the completion of a first read command, step (b) sets the parameters for a subsequent read command, and step (c) is the start of the subsequent read command. Note also that data is read over bus 16 and the registers are updated via bus 16.

Asano fails to teach the controller chip having direct memory access (DMA) controller, the DMA controller operatively coupled to the memory.

Taniai teaches a DMA controller that provides data via a bus, updates registers via a bus, and provides data via the bus responsive to the update (see lines 6-32 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Asano with the above teachings of Taniai. One of

ordinary skill in the art would have been motivated to make such modification in order to relieve the processor of the burdensome task of transferring data.

Allowable Subject Matter

21. Claims 6-14 are allowed.

Response to Arguments

22. Applicant's arguments with respect to claims 1-5 and 15-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on 571-272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJS
February 2, 2008

Eric Sond 2/2/08

APPROVED: /ES/

02/02/2008

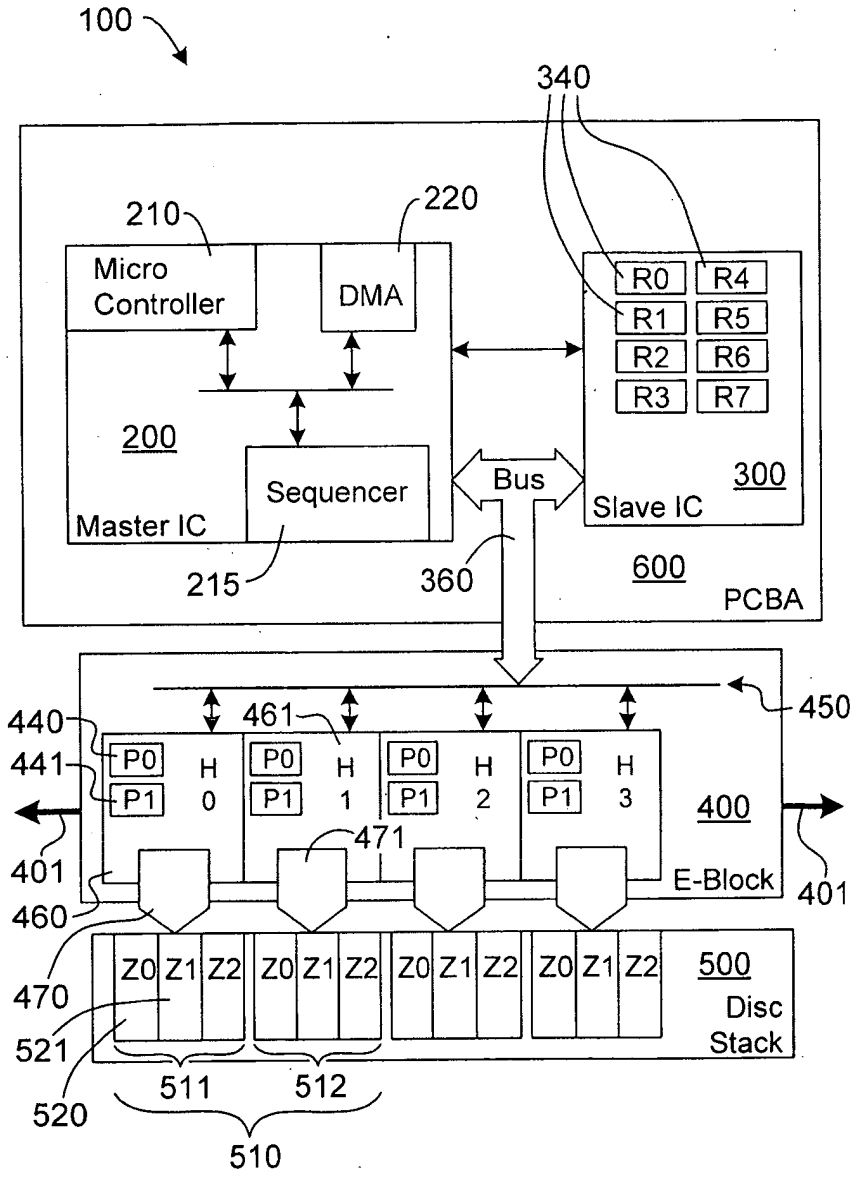

Fig. 3